REMARKS

The Office Action dated January 31, 2005, has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claims 1 and 7 are amended to more particularly point out and distinctly claim the subject matter of the invention. Support for the changes to claims 1 and 7 may be found in the specification, for example, on page 99, line 6 to page 100, line 32. No new matter is added by these amendments and no further consideration and/or search is needed. Thus, claims 1-7 are pending in the present application, and are respectfully submitted for consideration.

Claims 1-2 and 7 were rejected under 35 U.S.C. §102(a) as allegedly being unpatentable over U.S. Patent No. 5,909,686 (*Muller et al.*) (hereinafter *Muller I*). The Office Action took the position that *Muller I* taught the elements of claims 1-2 and 7. Applicants submit that the cited reference of *Muller I* does not disclose or suggest all the features of any of the presently pending claims.

Claim 1, upon which claim 2 is dependent, recites a network switch stack configuration. The configuration includes a first network switch comprising a plurality of data ports, a first stacking port, a first internet port interface controller, and a first CPU interface. The configuration also includes a set network switch having a plurality of data ports, a second stacking port, a second internet port interface controller, and a second CPU interface. The configuration also includes a common CPU connected to the first

CPU interface and the second CPU interface. The first stacking port and the second stacking port are communicatively connected through the first and second internet port interface controllers, such that incoming packets on any of the plurality of data ports on the first and second switches are effectively switched to any of the plurality of data ports on either of the first and second network switches. The first and second switches add module headers having module fields to the incoming packets and the first and second stacking ports read the module headers to determine egress ports for the packets.

Claim 7 recites a method for routing packets in a network switch stack configuration. The method includes communicatively connecting a first stacking port and a second stacking port. A first network switch includes the first stacking port and a second network switch includes the second stacking port. The method also includes adding module headers having module header fields to incoming packets on any of a plurality of data ports by the first and second switches. The method also includes reading the module headers by the first and second stacking ports to determine egress ports for the incoming packets. The method also includes switching the incoming packets to the egress ports via at least one internet port interface controller. The egress ports include any of the plurality of data ports on either of the first and second network switches.

As discussed in the specification, examples of the present invention enable incoming packets on any of a plurality of data ports on a first a second switches to be effectively switched to any of a plurality of data ports on either of the first and second network switches. Increased functionality is provided with respect to interconnectability.

In particular, examples of the present invention enable an increased amount of flexibility and performance regarding the stacking of a plurality of chips. It is respectfully submitted that the cited reference fails to disclose or suggest the elements of any of the presently pending claims. Therefore, the cited reference fails to provide the critical and unobvious advantages discussed above.

Muller I relates to hardware assisted central processing unit access to a forwarding database. A switch fabric provides access to a forwarding database on behalf of a processor, and includes a memory access interface configured to arbitrate access to a forwarding database memory. *Muller I* describes a generic packet header 499 that is partitioned into four portions, an L2 header portion 475, an L2 encapsulation portion 480, an L3 address independent portion 485, and an L3 address dependent portion 490. A subsystem 110 of *Muller I* includes a switch element 100 coupled to forwarding and filtering database 140. Optional cascading interface 225 of switch element 100 interconnects switching elements to create larger switches. CPU 161 transmits commands to network switch element 100 via CPU interface 215. Input packet processing is performed by one or more input ports of network interface 205, such as receiving and verifying Ethernet packets and transferring an incoming packet to shared memory manager 220 for storage in external shared memory 230.

Applicants submit that the cited reference does not disclose or suggest all the features of any of the presently pending claims. For example, Applicants submit that *Muller I* does not disclose or suggest "the first stacking port and the second stacking port

are communicatively connected through said first and second internet port interface controllers, such that incoming packets on any of the plurality of data ports on the first and second switches are effectively switched to any of the plurality of data ports on either of the first and second network switches," as recited in claim 1. Claim 7 recites "switching said incoming packets to said egress ports via at least one internet port interface controller." Applicants submit that the cited reference does not disclose or suggest at least these features of the pending claims.

Applicants further submit that *Muller I* does not disclose or suggest a first and a second internet port interface controllers. *Muller I* describes using various interfaces in its switch element, but none of these disclose or suggest an internet port interface controller. None of the interfaces of *Muller I* discloses or suggests connecting switches and switching incoming packets on any of the plurality of data ports on the switches to any of the plurality of data ports on either switch. For example, the network interface 205 of *Muller I* receives and verifies incoming Ethernet packets, and then possibly stores the packet. This aspect of *Muller I* does not disclose or suggest switching an incoming packet on the ports of a first or second switch to output on the ports on the first or second switch. In contrast, an internet port interface controller, as claimed, may switch incoming packets to an egress port on a first or second switch. For example, an internet port interface controller may switch an incoming packet of a first switch to an egress port on a second switch. *Muller I* does not disclose or suggest at least these features of the pending claims. Therefore, applicants request that the anticipation rejection be withdrawn.

Claims 3-6 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Muller I* in view of U.S. Patent No. 6,119,196 (hereinafter *Muller II*). The Office Action took the position that *Muller I* taught all the elements of claims 3-6 except that "the cascading interface 225 includes an arbiter for allocating communication bandwidth between the first and second stacking port[s], and a flow control logic for controlling data flow to and from each of the first and second network switches." The Office Action then alleged that *Muller II* provided those elements missing from *Muller I*. Applicants submit that the cited references of *Muller I* and *Muller II*, either alone or in combination, do not disclose or suggest all the features of the presently pending claims.

Claims 3-6 depend from claim 1. Claim 1 is summarized above. Applicants submit that claims 3-6 recite the patentable features of claim 1, and are allowable over *Muller I* and *Muller II*.

Muller II relates to a method and apparatus for managing a buffer memory in a packet switch that is shared between multiple ports in a network system. *Muller II* describes an apparatus that has a plurality of slow data port interfaces configured to transmit data at a first data rate between a slow data port. *Muller II* also describes a buffer memory and a plurality of fast data port interfaces configured to transmit data at a second data rate between a fast data port and a buffer memory. A first level arbiter is coupled to the plurality of slow data port interfaces, where the first level arbiter chooses an access request of one of the slow data ports and outputs the access request.

The Office Action concedes that *Muller I* does not teach all the features of claims 3-6. Applicants also submit that *Muller II*, alone or in combination with *Muller I*, does not disclose or suggest all the features of claims 3-6. For example, applicants submit that the cited references do not disclose or suggest "the first stacking port and the second stacking port are communicatively connected through said first and second internet port interface controllers, such that incoming packets on any of the plurality of data ports on the first and second switches are effectively switched to any of the plurality of data ports on either of the first and second network switches," as recited in claims 3-6.

Muller II does not disclose or suggest an internet port interface controller, as claimed. Instead, *Muller II* describes managing a shared buffer memory between multiple ports. The buffer memory of *Muller II* does not disclose or suggest switching incoming packets to any of a plurality of ports on first and second switches. *Muller II* describes determining first and second data rates to transmit data between ports. This aspect of *Muller II* does not disclose or suggest the features of claims 3-6 missing from *Muller I*. Thus, applicants submit that the cited references, either alone or in combination, do not disclose or suggest all the features of any of the present pending claims.

Further, applicants submit that claims 3-6 are allowable over the cited references because claim 1 is nonobvious. If an independent claim is nonobvious, then any claim depending therefrom also is nonobvious. MPEP 2143.03. For at least these reasons,

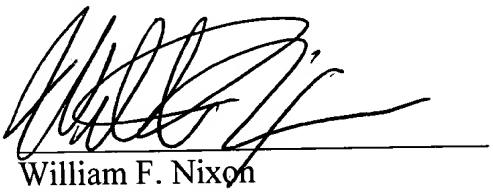
applicants submit that claims 3-6 are allowable over the cited references. Applicants respectfully request that the obviousness rejection of claims 3-6 be withdrawn.

It is respectfully submitted that each of claims 1-7 recite subject matter that is neither disclosed nor suggested by the cited references, either alone or in combination. It is therefore respectfully requested that all of claims 1-7 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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